



CYPRESS

CY7C199

32K x 8 Static RAM

Features

- High speed
 - 10 ns
- Fast t_{DOE}
- CMOS for optimum speed/power
- Low active power
 - 467 mW (max, 12 ns "L" version)
- Low standby power
 - 0.275 mW (max, "L" version)
- 2V data retention ("L" version only)
- Easy memory expansion with CE and OE features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

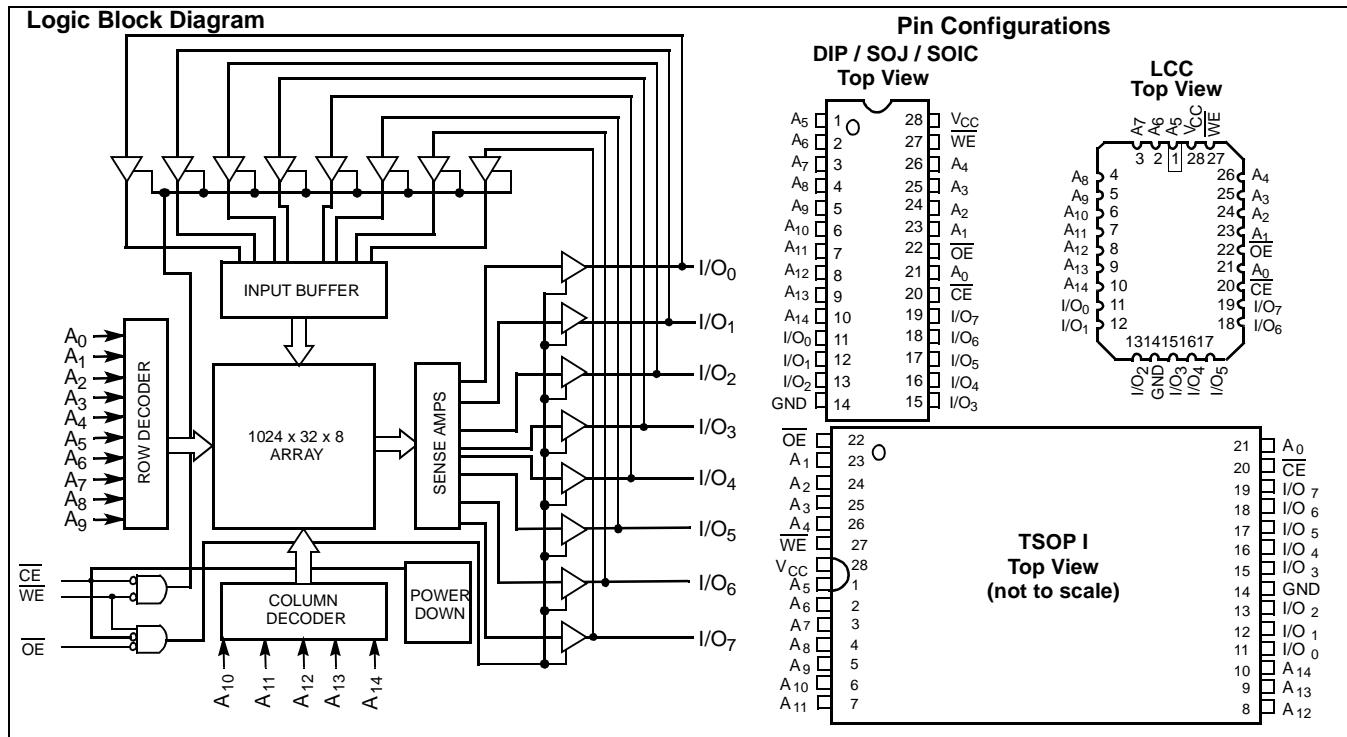
Functional Description

The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion

is provided by an active LOW Chip Enable (CE) and active LOW Output Enable (OE) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW Write Enable signal (WE) controls the writing/reading operation of the memory. When CE and WE inputs are both LOW, data on the eight data input/output pins (I/O₀ through I/O₇) is written into the memory location addressed by the address present on the address pins (A₀ through A₁₄). Reading the device is accomplished by selecting the device and enabling the outputs, CE and OE active LOW, while WE remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable (WE) is HIGH. A die coat is used to improve alpha immunity.



Selection Guide

	7C199 -8	7C199 -10	7C199 -12	7C199 -15	7C199 -20	7C199 -25	7C199 -35	7C199 -45	Unit
Maximum Access Time	8	10	12	15	20	25	35	45	ns
Maximum Operating Current	120	110	160	155	150	150	140	140	mA
L		90	90	90	90	80	70		
Maximum CMOS Standby Current	0.5	0.5	10	10	10	10	10	10	mA
L		0.05	0.05	0.05	0.05	0.05	0.05	0.05	

Shaded area contains advance information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage to Ground Potential (Pin 28 to Pin 14) -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs in High-Z State^[1] -0.5V to $V_{\text{CC}} + 0.5\text{V}$

DC Input Voltage^[1] -0.5V to $V_{\text{CC}} + 0.5\text{V}$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage $> 2001\text{V}$ (per MIL-STD-883, Method 3015)

Latch-up Current $> 200\text{ mA}$

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Industrial	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Military	-55°C to $+125^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range (-8, -10, -12, -15)^[3]

Parameter	Description	Test Conditions	7C199-8		7C199-10		7C199-12		7C199-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{\text{CC}} = \text{Min.}$, $I_{\text{OH}} = -4.0\text{ mA}$	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{\text{CC}} = \text{Min.}$, $I_{\text{OL}} = 8.0\text{ mA}$		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{\text{CC}} + 0.3\text{V}$	2.2	$V_{\text{CC}} + 0.3\text{V}$	2.2	$V_{\text{CC}} + 0.3\text{V}$	2.2	$V_{\text{CC}} + 0.3\text{V}$	V
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$\text{GND} \leq V_{\text{I}} \leq V_{\text{CC}}$	-5	+5	-5	+5	-5	+5	-5	+5	μA
I_{OZ}	Output Leakage Current	$\text{GND} \leq V_{\text{O}} \leq V_{\text{CC}}$, Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{\text{CC}} = \text{Max.}$, $I_{\text{OUT}} = 0\text{ mA}$, $f = f_{\text{MAX}} = 1/t_{\text{RC}}$	Com'l		120		110		160		155 mA
			L				85		85		100 mA
			Mil								180 mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	$\text{Max. } V_{\text{CC}}, \text{CE} \geq V_{\text{IH}}, V_{\text{IN}} \geq V_{\text{IH}}$ or $V_{\text{IN}} \leq V_{\text{IL}}, f = f_{\text{MAX}}$	Com'l		5		5		30		30 mA
			L				5		5		5 mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	$\text{Max. } V_{\text{CC}}, \text{CE} \geq V_{\text{CC}} - 0.3\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.3\text{V}$ or $V_{\text{IN}} \leq 0.3\text{V}, f = 0$	Com'l		0.5		0.5		10		10 mA
			L		0.05		0.05		0.05		0.05 mA
			Mil								15 mA

Electrical Characteristics Over the Operating Range (-20, -25, -35, -45) ^[3]

Parameter	Description	Test Conditions	7C199-20		7C199-25		7C199-35		7C199-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{\text{CC}} = \text{Min.}$, $I_{\text{OH}} = -4.0\text{ mA}$	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{\text{CC}} = \text{Min.}$, $I_{\text{OL}} = 8.0\text{ mA}$		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{\text{CC}} + 0.3\text{V}$	V						
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$\text{GND} \leq V_{\text{I}} \leq V_{\text{CC}}$	-5	+5	-5	+5	-5	+5	-5	+5	μA
I_{OZ}	Output Leakage Current	$\text{GND} \leq V_{\text{O}} \leq V_{\text{CC}}$, Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{\text{CC}} = \text{Max.}$, $I_{\text{OUT}} = 0\text{ mA}$, $f = f_{\text{MAX}} = 1/t_{\text{RC}}$	Com'l		150		150		140		140 mA
			L		90		80		70		70 mA
			Mil		170		150		150		150 mA

Shaded area contains advance information.

Notes:

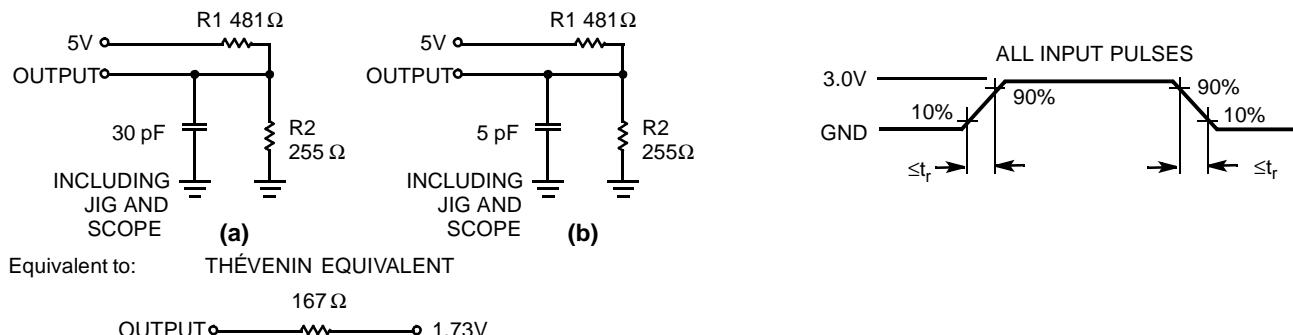
1. $V_{\text{IL}}(\text{min.}) = -2.0\text{V}$ for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.

Electrical Characteristics Over the Operating Range (-20, -25, -35, -45) (continued)^[3]

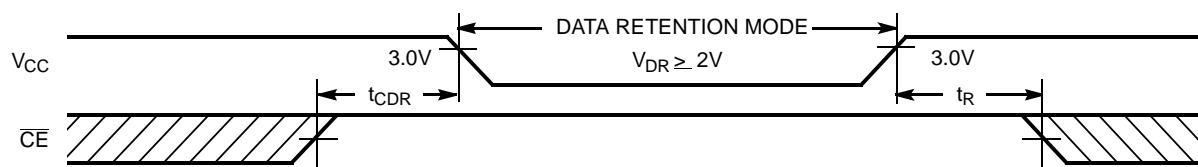
Parameter	Description	Test Conditions	7C199-20		7C199-25		7C199-35		7C199-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. $V_{CC}, CE \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	Com'l	30		30		25		25	mA
			L		5		5		5		mA
I _{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{CC} , $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f=0$	Com'l	10		10		10		10	mA
			L	0.05		0.05		0.05		0.05	µA
			Mil		15		15		15		mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1$ MHz, $V_{CC} = 5.0V$	8	pF
C _{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms^[5]

Data Retention Characteristics Over the Operating Range (L-version only)

Parameter	Description	Conditions ^[6]	Min.	Max.	Unit
V _{DR}	V _{CC} for Data Retention		2.0		V
I _{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$			µA
				10	µA
t _{CDR} ^[4]	Chip Deselect to Data Retention Time		0		ns
t _R ^[5]	Operation Recovery Time		200		µs

Data Retention Waveform

Note:

4. Tested initially and after any design or process changes that may affect these parameters.
5. $t_R \leq 3$ ns for the -12 and the -15 speeds. $t_R \leq 5$ ns for the -20 and slower speeds
6. No input may exceed $V_{CC} + 0.5V$.

Switching Characteristics Over the Operating Range (-8, -10, -12, -15) [3, 7]

Parameter	Description	7C199-8		7C199-10		7C199-12		7C199-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	CE LOW to Data Valid		8		10		12		15	ns
t_{DOE}	OE LOW to Data Valid		4.5		5		5		7	ns
t_{LZOE}	OE LOW to Low-Z ^[8]	0		0		0		0		ns
t_{HZOE}	OE HIGH to High-Z ^[8, 9]		5		5		5		7	ns
t_{LZCE}	CE LOW to Low-Z ^[8]	3		3		3		3		ns
t_{HZCE}	CE HIGH to High-Z ^[8, 9]		4		5		5		7	ns
t_{PU}	CE LOW to Power-up	0		0		0		0		ns
t_{PD}	CE HIGH to Power-down		8		10		12		15	ns
Write Cycle ^[10, 11]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	CE LOW to Write End	7		7		9		10		ns
t_{AW}	Address Set-up to Write End	7		7		9		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		ns
t_{PWE}	WE Pulse Width	7		7		8		9		ns
t_{SD}	Data Set-up to Write End	5		5		8		9		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	WE LOW to High-Z ^[9]		5		6		7		7	ns
t_{LZWE}	WE HIGH to Low-Z ^[8]	3		3		3		3		ns

Switching Characteristics Over the Operating Range (-20, -25, -35, -45) [3, 7]

Parameter	Description	7C199-20		7C199-25		7C199-35		7C199-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	20		25		35		45		ns
t_{AA}	Address to Data Valid		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	CE LOW to Data Valid		20		25		35		45	ns
t_{DOE}	OE LOW to Data Valid		9		10		16		16	ns
t_{LZOE}	OE LOW to Low-Z ^[8]	0		0		0		0		ns
t_{HZOE}	OE HIGH to High-Z ^[8, 9]		9		11		15		15	ns
t_{LZCE}	CE LOW to Low-Z ^[8]	3		3		3		3		ns
t_{HZCE}	CE HIGH to High-Z ^[8, 9]		9		11		15		15	ns
t_{PU}	CE LOW to Power-up	0		0		0		0		ns

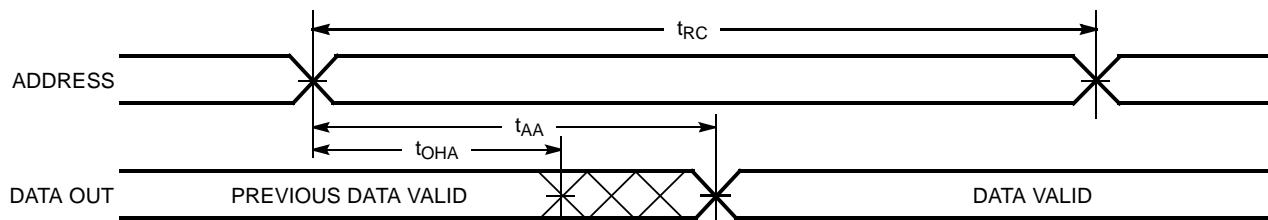
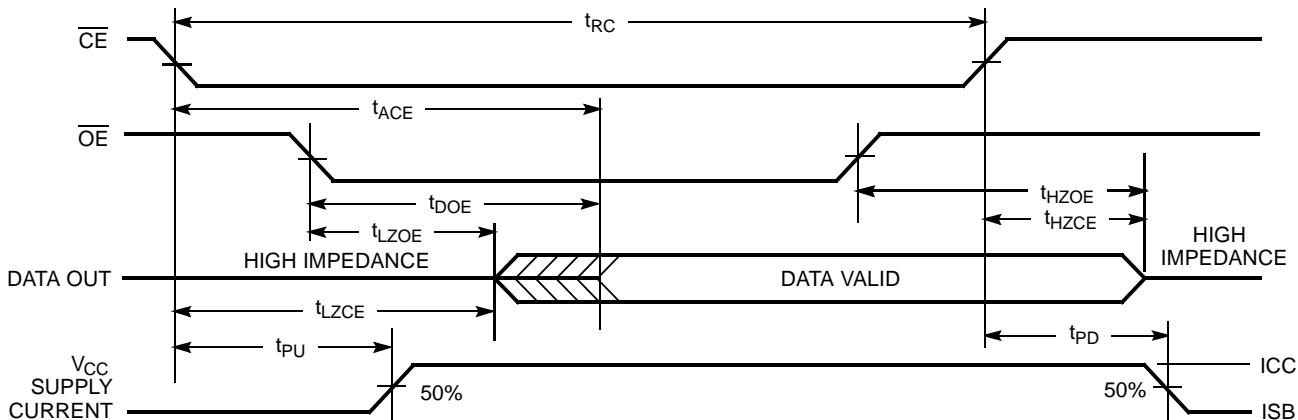
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Notes:

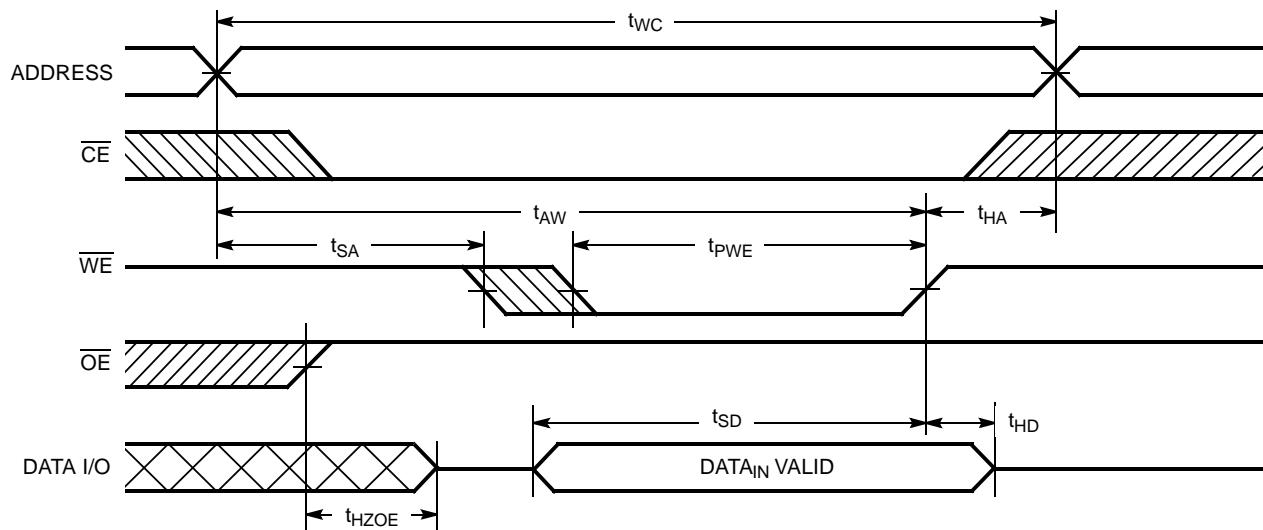
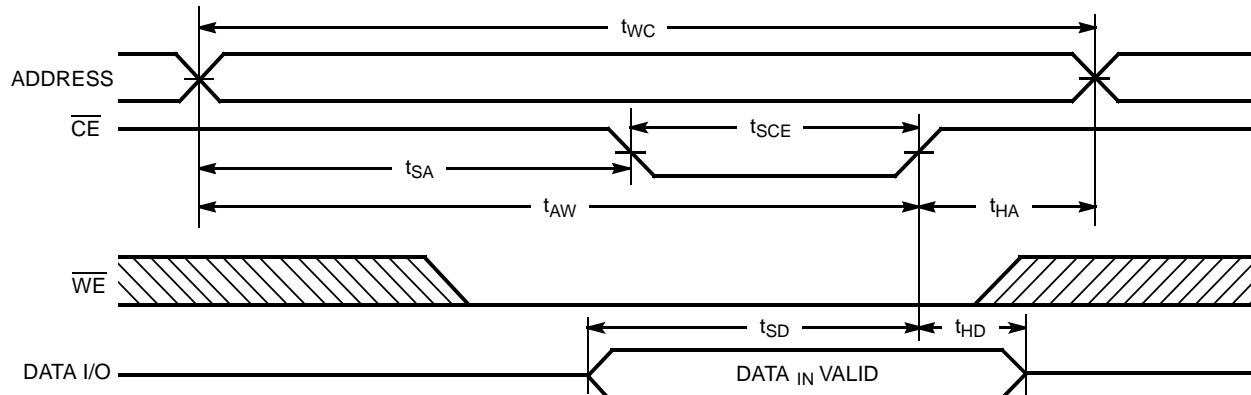
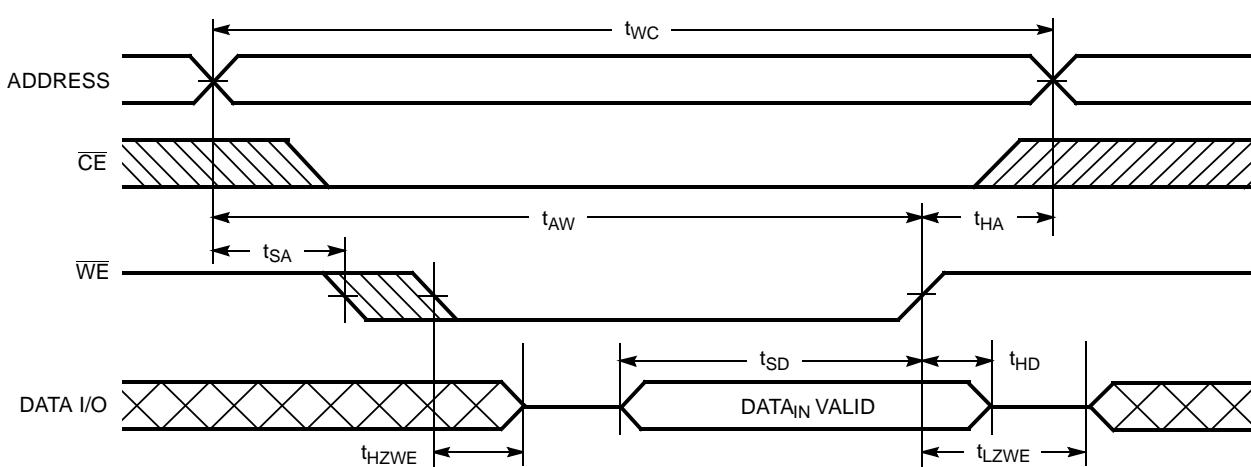
7. Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Characteristics Over the Operating Range (-20, -25, -35, -45)^[3, 7]

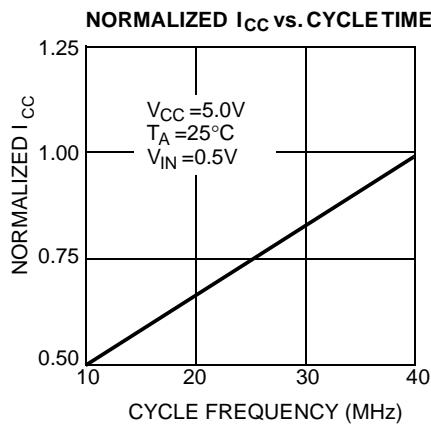
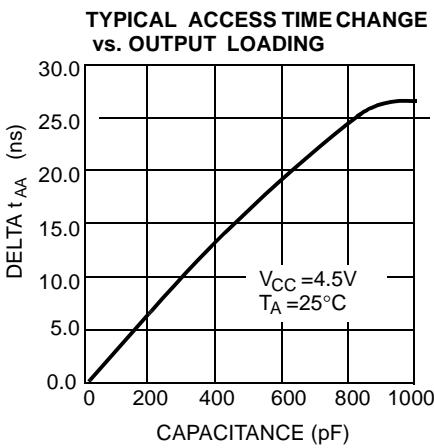
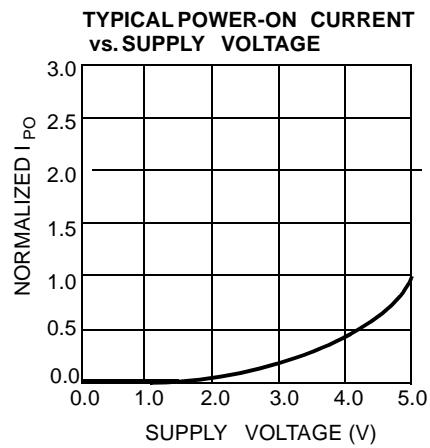
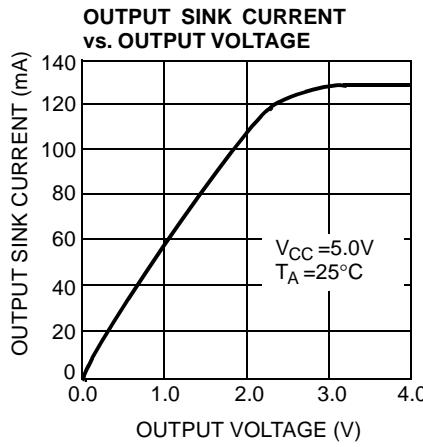
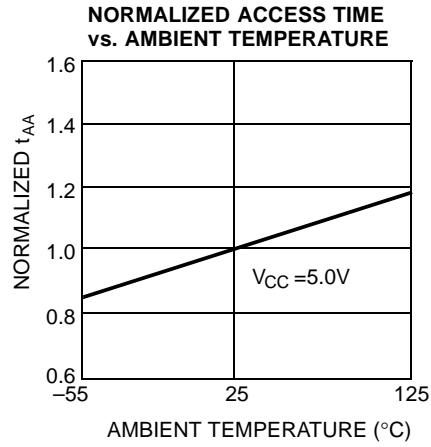
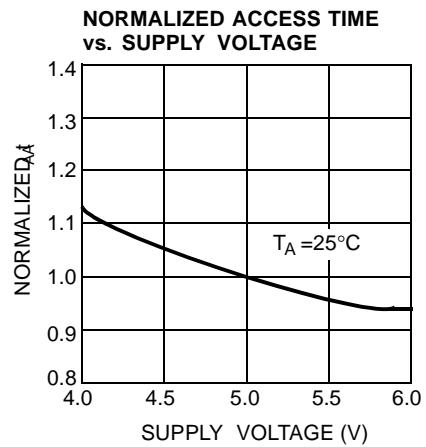
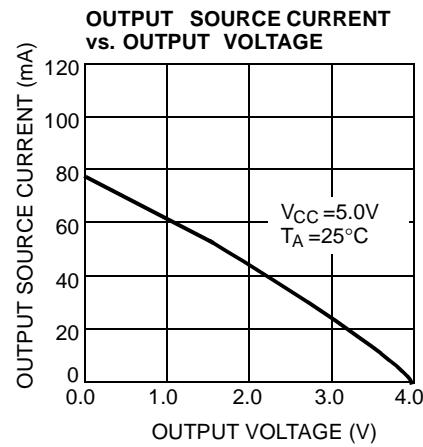
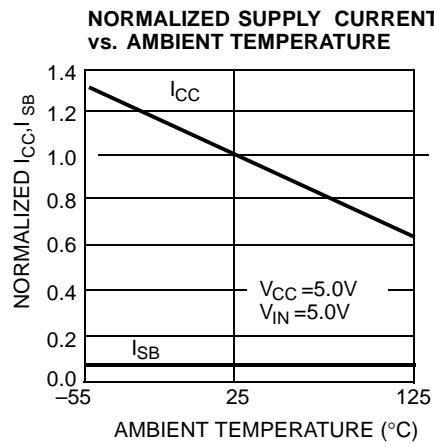
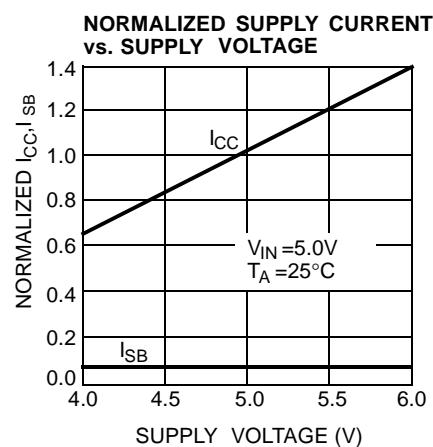
Parameter	Description	7C199-20		7C199-25		7C199-35		7C199-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	CE HIGH to Power-down		20		20		20		25	ns
Write Cycle^[10,11]										
t_{WC}	Write Cycle Time	20		25		35		45		ns
t_{SCE}	CE LOW to Write End	15		18		22		22		ns
t_{AW}	Address Set-up to Write End	15		20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		ns
t_{PWE}	WE Pulse Width	15		18		22		22		ns
t_{SD}	Data Set-up to Write End	10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	WE LOW to High-Z ^[9]		10		11		15		15	ns
t_{LZWE}	WE HIGH to Low-Z ^[8]	3		3		3		3		ns

Switching Waveforms
Read Cycle No. 1^[12, 13]

Read Cycle No. 2^[13, 14]

Notes:

12. Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} .
13. \overline{WE} is HIGH for read cycle.
14. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (WE Controlled)^[10, 15, 16]

Write Cycle No. 2 (CE Controlled)^[10, 15, 16]

Write Cycle No. 3 (WE Controlled OE LOW)^[11, 16]

Notes:

15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
16. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (Isb)
L	H	L	Data Out	Read	Active (Icc)
L	L	X	Data In	Write	Active (Icc)
L	H	H	High Z	Deselect, Output disabled	Active (Icc)

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C199-8VC	V21	28-Lead Molded SOJ	Commercial
	CY7C199-8ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-8VC	V21	28-Lead Molded SOJ	
	CY7C199L-8ZC	Z28	28-Lead Thin Small Outline Package	
10	CY7C199-10VC	V21	28-Lead Molded SOJ	Commercial
	CY7C199-10ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-10VC	V21	28-Lead Molded SOJ	
	CY7C199L-10ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-10VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199-10ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-10VI	V21	28-Lead Molded SOJ	
	CY7C199L-10ZI	Z28	28-Lead Thin Small Outline Package	
12	CY7C199-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-12VC	V21	28-Lead Molded SOJ	
	CY7C199-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199L-12VC	V21	28-Lead Molded SOJ	
	CY7C199L-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-12VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199-12ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-12VI	V21	28-Lead Molded SOJ	
	CY7C199L-12ZI	Z28	28-Lead Thin Small Outline Package	
15	CY7C199-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-15VC	V21	28-Lead Molded SOJ	
	CY7C199-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199L-15VC	V21	28-Lead Molded SOJ	
	CY7C199L-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-15VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199-15ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-15DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199L-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C199-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-20VC	V21	28-Lead Molded SOJ	
	CY7C199-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199L-20VC	V21	28-Lead Molded SOJ	
	CY7C199L-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-20VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199-20ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-20DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199L-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advance information. Contact your Cypress sales representative for availability

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C199-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-25SC	S21	28-Lead Molded SOIC	
	CY7C199-25VC	V21	28-Lead Molded SOJ	
	CY7C199-25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-25SI	S21	28-Lead Molded SOIC	Industrial
	CY7C199-25VI	V21	28-Lead Molded SOJ	
	CY7C199-25ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
35	CY7C199-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-35SC	S21	28-Lead Molded SOIC	
	CY7C199-35VC	V21	28-Lead Molded SOJ	
	CY7C199-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-35SI	S21	28-Lead Molded SOIC	Industrial
	CY7C199-35VI	V21	28-Lead Molded SOJ	
	CY7C199-35ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
45	CY7C199-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
	CY7C199-45DMB	D22	28-Lead (300-Mil) CerDIP	

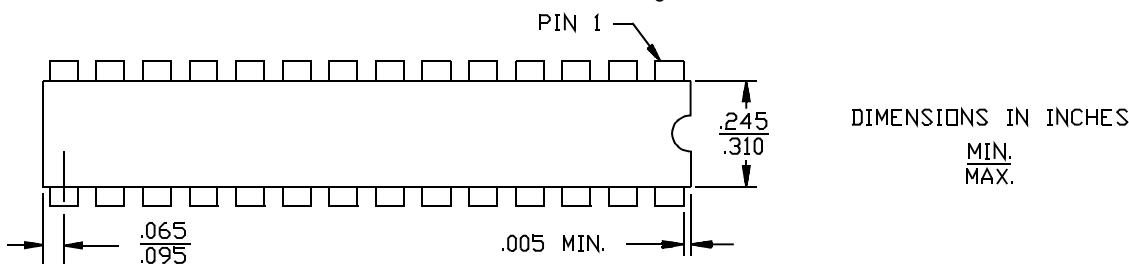
Shaded area contains advance information. Contact your Cypress sales representative for availability

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

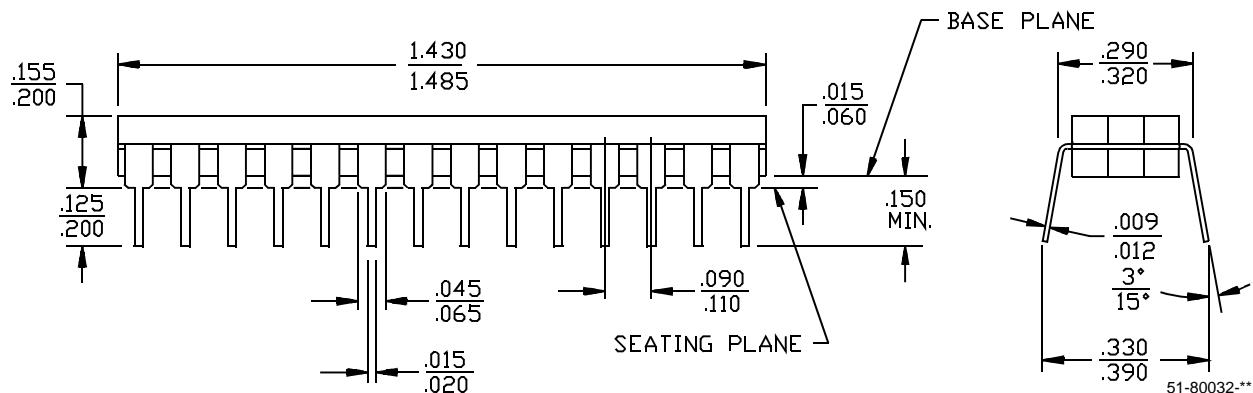
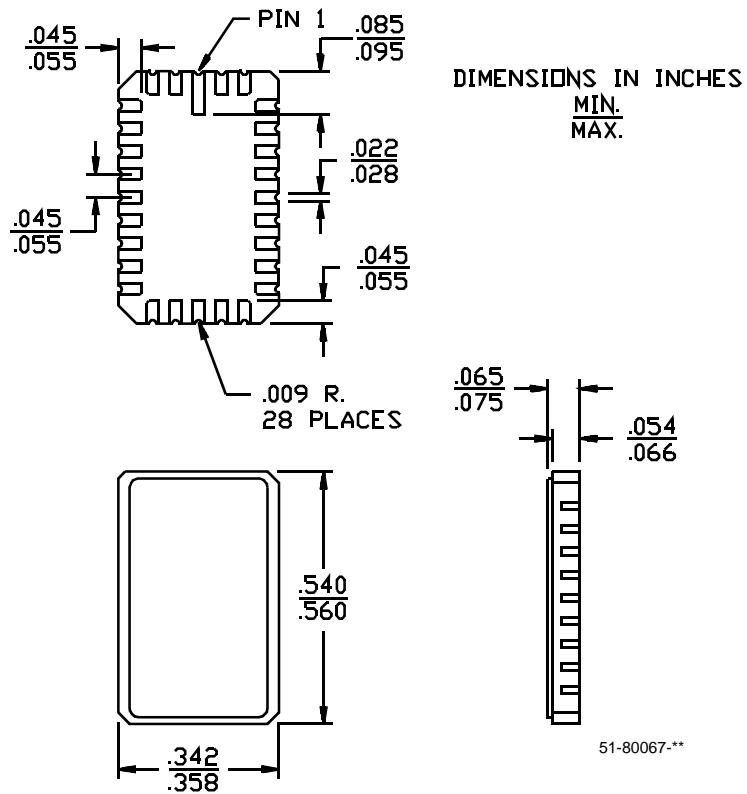
Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

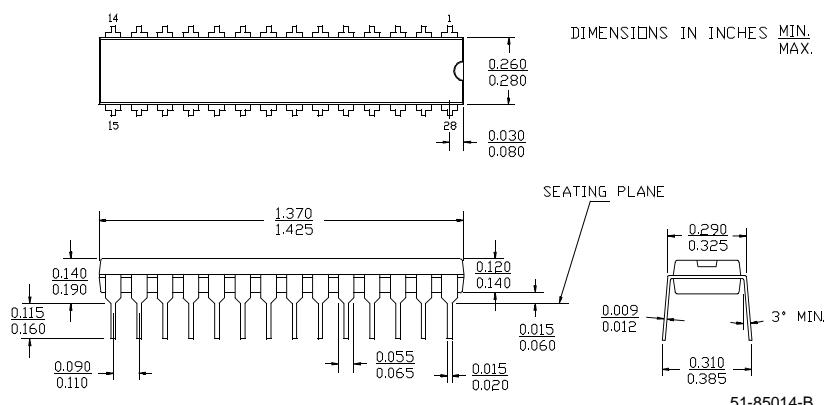
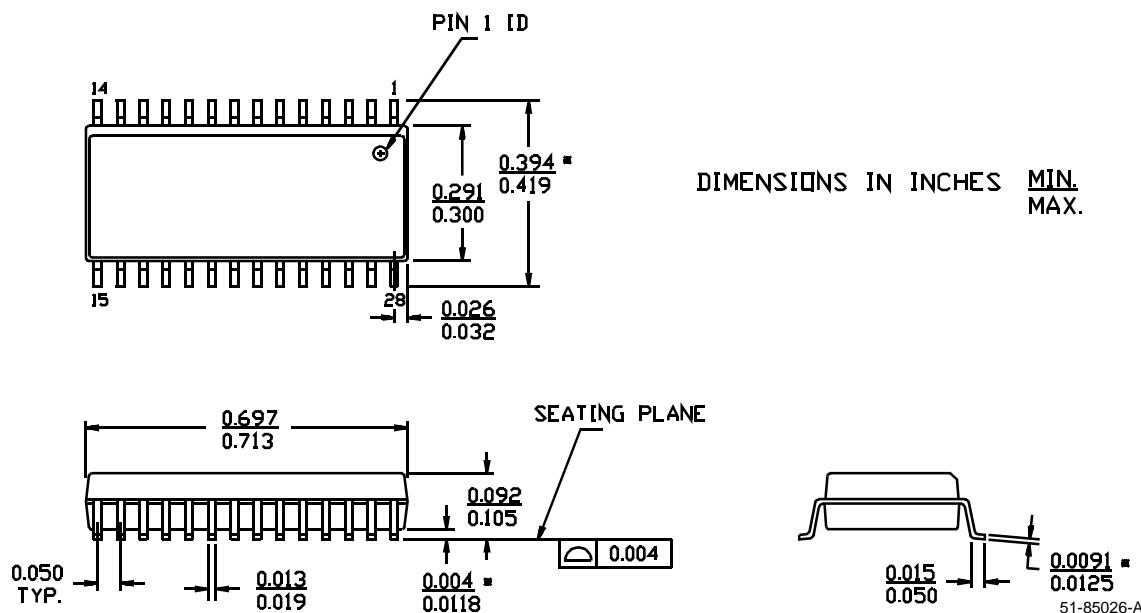
Switching Characteristics

Parameter	Subgroups
Read Cycle	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
Write Cycle	
t_{WC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Package Diagrams
28-pin (300-Mil) CerDIP D22
MIL-STD-1835 D-15 Config. A


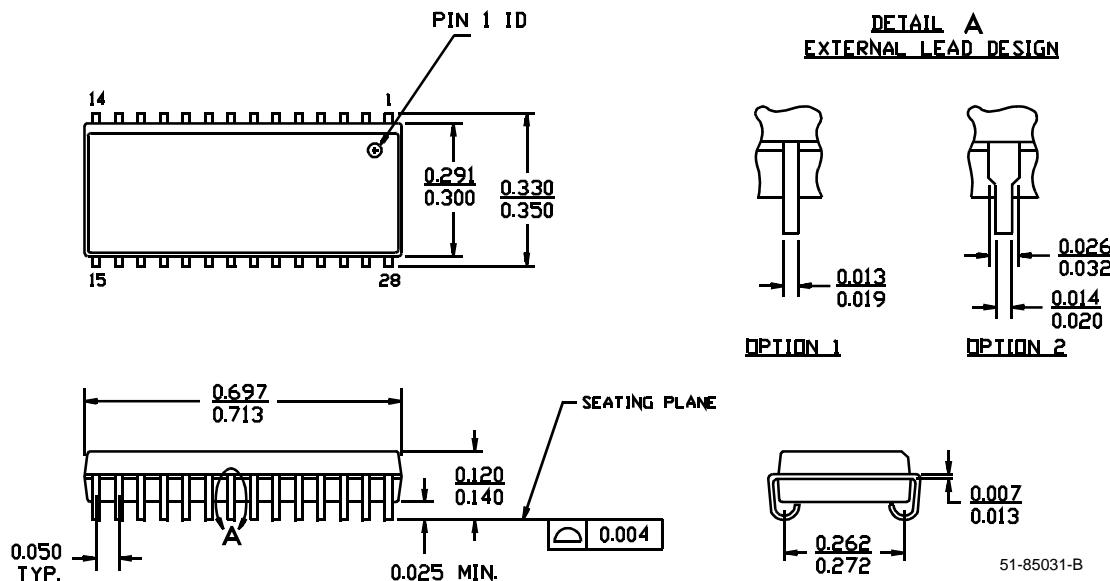
DIMENSIONS IN INCHES
MIN.
MAX.


28-pin Rectangular Leadless Chip Carrier L54
MIL-STD-1835C-11A


Package Diagrams (continued)
28-pin (300-Mil) Molded DIP P21

28-pin (300-Mil) Molded SOIC S21


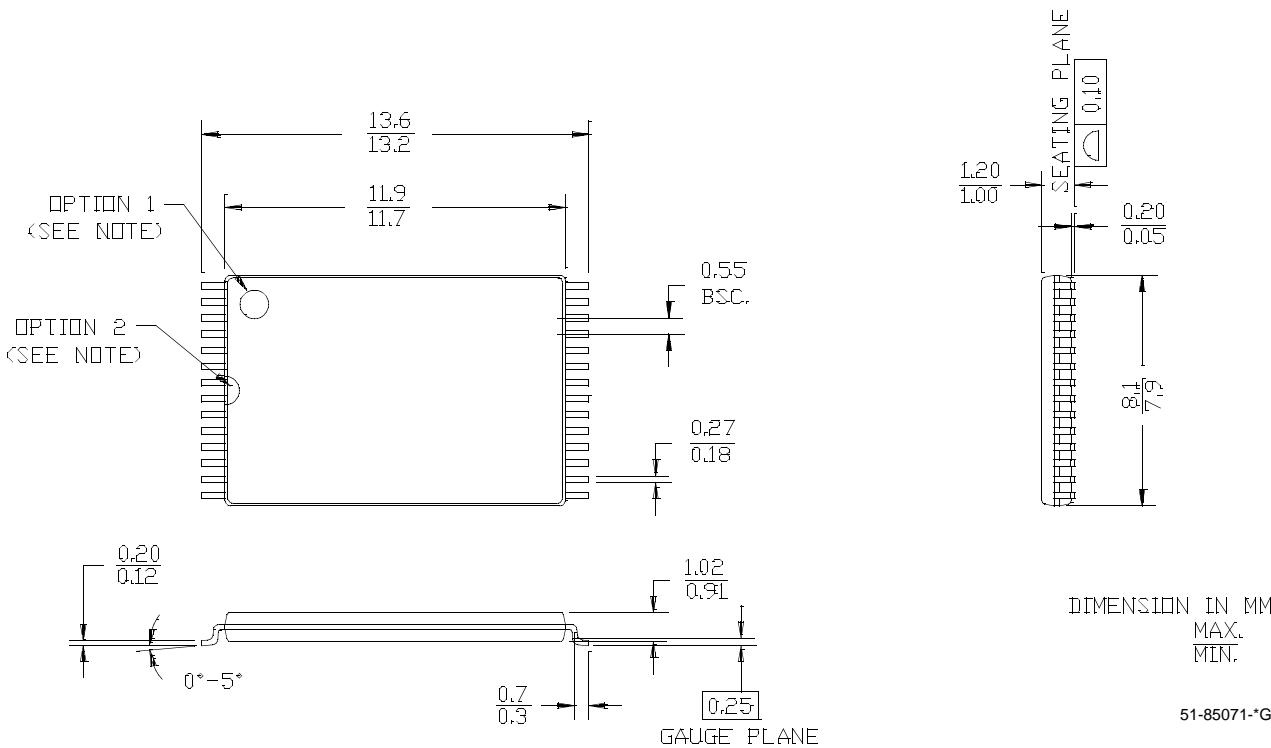
Package Diagrams (continued)

28-pin (300-Mil) Molded SOJ V21
DIMENSIONS IN INCHES **MIN.** **MAX.**



28-Lead Thin Small Outline Package Type 1 (8x13.4 mm) Z28

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



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Document History Page

Document Title: CY7C199 32K x 8 Static RAM Document Number: 38-05160				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109971	10/28/01	SZV	Change from Spec number: 38-00239 to 38-05160
*A	121730	01/09/02	DFP	Updated Product Offering table.